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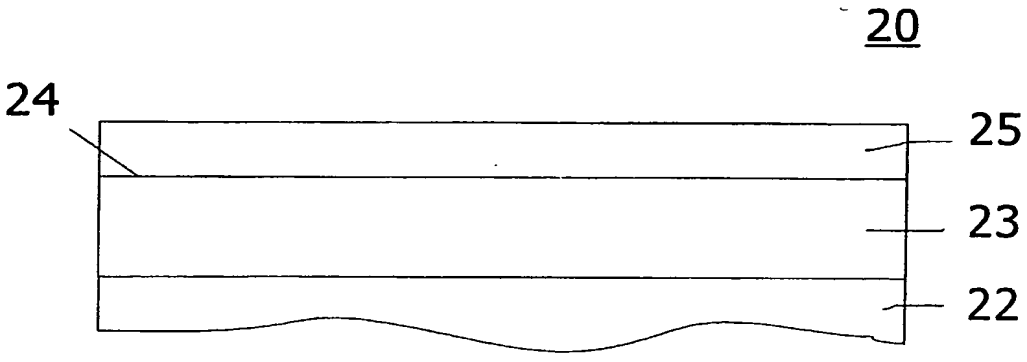
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: EPITAXIAL WAFER APPARATUS



(57) Abstract: A system (30) for coating the surface of compound semiconductor wafers includes providing a single-wafer epitaxial production system in a cluster-tool architecture with a loading (33), storage (34), and transfer (32) modules, a III-V deposition chamber, and an insulator deposition chamber. The compound semiconductor wafer (10) is placed in the loading and transfer module and the pressure is reduced to less than 5 x 10^{-10} Torr, after which the wafer is moved to the III-V growth chamber (35) and layers of compound semiconductor material are epitaxially grown on the surface of the wafer. The single wafer is then moved through the transfer module to the insulator deposition chamber and an insulating cap layer is formed by thermally evaporating molecules, consisting essentially of gallium and oxygen, from an effusion cell using a thermal evaporation source that utilizes a metallic iridium crucible that is manufactured using the electroforming process.

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EPITAXIAL WAFER APPARATUS

FIELD OF THE INVENTION

The present invention pertains to III-V semiconductor wafer coating and manufacturing and more specifically to surface protection of III-V compound semiconductor structures.

BACKGROUND OF THE INVENTION

The prior art in III-V epitaxial wafer technology employs a semiconductor layer as the top layer in a compound semiconductor epitaxial layer structure including, for example GaAs, $In_{1-x}Ga_xAs$, $In_{1-y}Ga_yP$, $Al_{1-x}Ga_xAs$, InGaAsP, InSb etc., depending on the specific device/circuit application and the particular compound semiconductor substrate. The use of a semiconducting top layers in prior epitaxial wafer technology results in a semiconductor surface structure that is easily oxidized upon exposure to the atmosphere. Since the oxidization and or contamination of the top layer of the semiconductor structure occurs immediately and uncontrollably upon exposing the compound semiconductor wafer to the oxygen, water vapor, hydrocarbons, and other chemicals in the atmosphere, the physical and electronic properties of the newly oxidized semiconductor structure are altered in an uncontrollable and unpredictable manner. After such contamination and oxidization, detrimental electrical and chemical surface properties are observed in compound semiconductor structures that have detrimental effects on electronic and optoelectronic properties that negatively effect the subsequent device and integrated circuit performance. The degree of complication and degradation of a particular device or integrated circuit is subject to the particular device/circuit processing and application. For example, the fabrication and performance of unipolar Field Effect Transistor devices/circuits may be deleteriously effected by atmospheric exposure, oxygen or water vapor exposure, or oxygen plasma exposure, that leads to Fermi level pinning, and also instability of the gate-source and

gate-drain regions. Since a high quality native oxide on GaAs and other III-V semiconductors cannot be formed by processes such as thermal oxidation or surface oxidation, the fabrication of useful and stable MOSFET devices has not been possible to date in GaAs or InP based semiconductors.

Uncontrollable and detrimental electrical and surface properties are caused by chemical surface reactions resulting in the formation of native oxides and dangling bonds on compound semiconductor interfaces. The surface is also rendered thermodynamically unstable after formation of the native oxide and exhibits a pinned Fermi level. More specifically, the high GaAs surface reactivity induces Fermi level pinning and surface instability after surface exposure as small as 10^5 Langmuirs (1 Langmuir=10^{-6} Torr). Surface preparation techniques conducted after exposure to air or oxygen including exposure to compounds and suspensions of sulfur and selenium, etc. have yielded compound semiconductor surfaces and interfaces that are unstable and not useful in the manufacturing of any type of GaAs integrated circuits and electronic or optoelectronic devices. Other Prior art, U.S. Pat. No. 5,451,548, entitled "Electron Beam Deposition of Gallium Oxide Thin Films using a Single Purity Crystal Layer", issued Sep. 19, 1995, and U.S. Pat. No. 5,550,089, entitled "Gallium Oxide Coatings for Optoelectronic Devices Using Electron Beam Evaporation of a High Purity Single Crystal Gd_3 Ga_5O_{12} Source", issued Aug. 27, 1996, reported that thermodynamically stable, III-V semiconductor surfaces and/or interfaces with low interface state density can be fabricated when a specific insulating cap layer is deposited in-situ on GaAs based semiconductor epitaxial layers using e-beam evaporation of $Gd_3Ga_5O_{12}$ while maintaining ultra-high vacuum (UHV). Other prior art, such as U.S. Pat. No. 6.030.453, 'III-V Epitaxial Wafer Production', issued Feb. 29, 2000 reports that gallium oxide layers on GaAs may be formed using Ga_2O_3 thermally evaporated from an oxide crucible fabricated from BeO and other oxide materials. However in our experience, the

resulting films containing gallium and oxygen produced from thermal evaporation using a high temperture effusion cell from a BeO crucible are heavily doped with Be that is known to be an impurity and dopant in GaAs that results in unreliable devices and unreliable integrated circuits. Furthermore since the resulting Be concentration can exceed $10^{21}cm^{-3}$, the resulting gallium oxide layers produced possess residual conductivity, and thus the resulting oxide films are not insulating in nature and character. A useful protective coating for GaAs must be free of impurities at concentrations below one part in $10^{19}cm^{-3}$, and more preferably completely free of impurities at levels below 1 part in $10^{16}cm^{-3}$. Furthermore, the resulting GaAs/coating interface must be formed at extremely low pressures to limit GaAs surface exposure to <10-100 Langmuirs of various impurities while simultaneously preserving the GaAs bulk and surface stoichiometry. The process described in both patents detailing the prior art is not useful or manufacturable because the previously disclosed processes produce coating layers that are laden with impurities that render the subsequent semiconductor devices and circuits essentially non-functional or unreliable in normal operation. Therefore, it would be highly advantageous to provide new methods of manufacturing such compound semiconductor insulator interfaces that overcome the limitations of the prior art.

It is a purpose of the present invention to provide a new and improved III-V epitaxial wafer production process that includes the placement of a useful protective, non-contaminating and passivating coating on the compound semiconductor surface.

It is another purpose of the present invention to provide a new and improved III-V epitaxial wafer with improved stability and reliability.

It is still another purpose of the present invention to provide a new and improved III-V wafer which is relatively easy to fabricate and use for semiconductor device manufacture in both the electronic and opto-electronic fields.

SUMMARY OF THE INVENTION

The above problems and others are at least partially solved and the above purposes and others are realized in a method of coating, protecting, and passivating the surface of a compound semiconductor wafer structure including the steps of providing a compound semiconductor wafer structure with a surface and forming a truly insulating cap layer on the surface of a compound semiconductor wafer structure by thermally evaporating insulating material onto the wafer structure provided that such evaporation occurs on an atomically clean compound semiconductor surface, in an ultra high vacuum environment, and using a polycrystalline Ga_2O_3 that is placed in a metallic Ir crucible that is clean, outgassed at temperatures in excess of 1700°C in a ultra high vacuum environment and conically shaped using the electro-forming process.

In this specific semiconductor production process, a single-wafer epitaxial production system is provided including, loading, transfer, and storage modules with a III-V growth chamber attached and a second insulator deposition chamber also attached to the centralized transfer module. A compound semiconductor wafer with polished surface is placed in the loading module and the pressure therein is reduced to $<10^{-6}$ Torr. The compound semiconductor wafer is moved through the transfer module to the III-V growth chamber where the base pressure is below 10^{-10} Torr and layers of compound semiconductor material are epitaxially grown on the surface of the compound semiconductor wafer. The compound semiconductor wafer is then moved to the transfer module and then immediately into the insulator chamber, while maintaining an ultra-high vacuum environment at all times. A subsequent insulating cap layer is formed by thermally evaporating Ga_2O_3 material from an electroformed Iridium crucible onto the layer topmost of compound semiconductor structure. This deposition process is complete when a layer consisting of gallium oxygen molecules is produced with high purity and atomic abruptness on the surface of the compound semiconductor.

BRIEF DESCRIPTION OF THE FIGURES

Referring to the figures:

FIG. 1, illustrates a simplified cross-sectional view of a prior art compound semiconductor substrate with a native oxide formation on the surface thereof;

FIG. 2 illustrates a simplified cross-sectional view of a compound semiconductor substrate with epitaxial and cap layers in accordance with the present invention;

FIG. 3 illustrates a single-wafer epitaxial production system with a centralized transfer module utilized in fabricating the structure of FIG. 2 in accordance with the present invention; and

FIG. 4 is a photograph of the Iridium metal crucible that is generally of a conical shape and has one closed end and one open end and has been fabricated utilizing the electroforming process.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring specifically to FIG. 1, a prior art III-V compound semiconductor wafer 10 is illustrated. Wafer 10 includes a substrate with one or more layers of III-V material epitaxially formed on the upper surface thereof. For purposes of this disclosure the substrate and any epitaxial layers formed thereon will be referred to simply as a compound semiconductor wafer structure, which in FIG. 1 is designated 12. Compound semiconductor wafer structure 12 has a top layer 13 with an upper surface 14. Any exposure of compound semiconductor wafer structure 12 or top layer 13 to oxygen, water vapor or ambient conditions (air, processing environments, etc.) results in a layer 15 of native oxide being formed on the surface. Generally, layer 15 is very thin, approximately 10 angstrom thick. The interface between top layer 13 and native oxide layer 15 is not atomically abrupt, and is thermodynamically unstable with a pinned Fermi level.

A compound semiconductor wafer structure 20 formed in accordance with the present invention is illustrated in FIG. 2. Compound semiconductor wafer structure 20 generally includes a compound semiconductor substrate with one or more layers of III-V material epitaxially formed on the upper surface thereof, hereafter designated 22. Compound semiconductor wafer structure 20 has a top layer 23 with an upper surface 24. It will of course be understood that in some specific applications (or on some portions of compound semiconductor wafer structure 20) there may be no epitaxial layers present on the substrate and upper surface 24 may simply be the upper surface of the substrate. An insulating cap layer 25 is thermally evaporated onto surface 24 of compound semiconductor wafer structure 20.

Turning now to FIG. 3, a single-wafer epitaxial production system 30 is illustrated, which is utilized in fabricating compound semiconductor wafer structure 20 of FIG. 2 in accordance with the present invention. System 30 includes a loading module 33, transfer module 32, storage module 34, a III-V growth chamber 35 attached to transfer module 33, and an insulator chamber 38 attached to the transfer module 33. Each of chambers 35 and 38 are attached to transfer and load module 33 so that wafers, chips, etc. can be processed in each chamber without removing the wafers, chips, etc. from the ultra-high vacuum environment of system 30. Therefore, once a wafer is introduced into system 30 and a vacuum is drawn, the wafer is not subjected to the ambient environment or oxygen exposure until the process is completed. Thus, as an example of a process of protecting the surface of a compound semiconductor wafer structure in accordance with the present invention, a compound semiconductor wafer is placed in loading module 31 and the pressure in loading module 31 is reduced to $<10^{-6}$ Torr. The wafer is then moved into the transfer module where the pressure is reduced to $< 10^{-9}$ Torr, and then into the III-V growth chamber 35 where the base pressure is $<10^{-10}$ Torr and one or more layers of compound semiconductor material are epitaxially

grown on the surface to produce a compound semiconductor wafer structure (e.g. compound semiconductor wafer structure 20). After the growth of top layer 23, compound semiconductor wafer structure 20 is moved to transfer module 33 and then to insulator chamber 38 while maintaining pressures below $5x10^{-10}$ Torr. Within insulator chamber 38, insulating cap layer 25 is formed on surface 24 of compound semiconductor wafer structure 20 by thermally evaporating Ga_2O_3 material from an electroformed Ir crucible onto wafer structure 20.

In a preferred embodiment of the process, insulating cap layer 25 is thermally evaporated onto surface 24 of wafer structure 20 that is first formed in an atomically abrupt manner in the III-V growth chamber 35 by thermally evaporating gallium oxide molecules from an effusion cell using a thermal evaporation source in a metallic Ir crucible that is generally conical in shape and has been fabricated using the electroforming process. The evaporation source may be pure Ga_2O_3 or may be composed of one of several Ga_2O_3 + rare earth element compounds or mixtures. In a second preferred embodiment the surface cotaing and protection layer that consists of primarily of gallium and oxgen compounds would be formed from the evaporation of crystalline gadolinium gallium garnet ($Ga_3Gd_5O_{12}$) from an electroformed Ir crucible. The metallic Ir crucible is generally of a conical shape, having one closed end and one open end and is fabricated using the electroforming process or chemical vapor deposition processes familiar to those skilled in the art. The crucible and effusion cell are further positioned in the insulator chamber in close proximity to the compound semiconductor wafer such that measurable deposition rates of gallium oxygen layers are achieved on the compound semiconductor structure at thermal evaporation temperatures below 1650°C at the crucible. The deposition rate of Ga_2O_3 onto the compound semiconductor structure under the most preferable conditions is approximately 0.01 to 0.02 angstroms per second.

After the deposition of an insulating cap layer 25 that is composed of approximately 10 angstroms of gallium oxygen molecules the compound semiconductor wafer structure 20 is protected from exposure to ambient conditions and contamination until insulating cap layer 25 is removed. Because insulating cap layer 25 is formed in system 30 of FIG. 3, the structure or epitaxial layers are never subjected to ambient conditions and the interface between the substrate or epitaxial layers and insulating cap layer 25 is thermodynamically stable with excellent electrical properties. In the specific example of a compound semiconductor wafer structure with a GaAs surface and a layer of oxide deposited thereon, the GaAs-Ga_2O_3 interface exhibits abruptness within a single atomic layer and the oxide has a surface roughness <2.0 angstom (rms). Also, it has been found that there is excellent uniformity of interface state density over a fabricated wafer. The interface state density is in general comparable or better than prior art densities (10^{10} cm^{-2} eV^{-1}).

The thermally evaporated insulating layer on the wafer structure of the disclosed process replaces the exposed semiconductor surface of prior art epitaxial products and the buried epitaxial semiconductor surface is electrically and chemically stable and exhibits excellent electrical properties. Thus, the improved compound semiconductor wafer structure fabricated in accordance with the novel surface protection process has the following advantages: excellent electrical and chemical properties, passivation and protection of the semiconductor epilayer structure and devices/circuits formed therein; stability of the excellent electronic and chemical surface properties of the semiconductor epilayer structure and devices/circuits formed therein; simplification of device/circuit processing; improved reproducibility and reliability of devices/circuits; and essential parts of the semiconductor surface are not exposed during processing, preserving electronic passivation.

These improvements essentially solve or overcome the problems of the prior art, such as poor reliability, dc electrical instability, and electrical hysterisis, and therefore provide a highly

manufacturable process. While we have shown and described specific embodiments of the present invention, further modifications and improvements will occur to those skilled in the art. We desire it to be understood, therefore, that this invention is not limited to the particular forms shown and we intend in the appended claims to cover all modifications that do not depart from the spirit and scope of this invention.

What is claimed:

1. A method of coating the surface of a compound semiconductor wafer structure with a protective and passivating layer consisting primarily of gallium and oxygen molecules in a layer including the steps of:

   a. providing a compound semiconductor substrate with compound semiconductor epitaxial structure with a surface;

   b. positioning a crystalline, high purity Ga_2O_3 evaporation source consisting essentially of only Ga_2O_3 placed into a metallic Iridium crucible that is generally of a conical shape with one open end and one closed end where said crucible has been fabricated using the electroforming or chemical vapor deposition process;

   c. forming a gallium oxygen layer on the surface of the wafer structure by thermally evaporating gallium oxide molecules from the crystalline, high purity Ga_2O_3 evaporation source onto the surface of the compound semiconductor wafer structure.

2. A method of protecting the surface of a semiconductor wafer comprising the steps of:

   a. providing a single-wafer epitaxial production system including a loading module, transfer module, storage module, and unloading module with both a III-V growth chamber attached and an insulator deposition chamber attached to said transfer module;

   b. providing a compound semiconductor substrate with a surface;

   c. placing the compound semiconductor substrate in the loading module;

   d. reducing the pressure in the loading module below 10^{-6} Torr;

   e. moving said wafer through the transfer module in the III-V deposition chambers;

   f. reducing the pressure in said III-V deposition chamber to $<10^{-10}$ Torr;

   g. epitaxially growing layers of compound semiconductor material on the surface of the compound semiconductor wafer;

   h. moving the compound semiconductor wafer to the transfer and load module and then to the insulator chamber;

   i. positioning a crystalline, high purity Ga_2O_3 evaporation source consisting essentially of only Ga_2O_3 placed into a metallic Iridium crucible that is generally of a conical shape with one open end and one closed end where said crucible has been fabricated using the electroforming or chemical vapor deposition process;

j. forming a gallium oxygen layer on the surface of the wafer structure by thermally evaporating gallium oxide molecules from the crystalline, high purity Ga_2O_3 evaporation source onto the surface of the compound semiconductor wafer structure;

k. forming an insulating cap layer by thermally evaporating gallium oxide molecules from the crystalline, high purity Ga_2O_3 evaporation source onto the layers of compound semiconductor material;

l. moving said compound semiconductor structure to the insulator chamber through the transfer chamber to the unloading module.

3. A method of protecting the surface of a semiconductor wafer as claimed in claim 2 wherein the step of providing the compound semiconductor wafer includes providing a compound semiconductor wafer of gallium-arsenide (GaAs).

4. A method of protecting the surface of a semiconductor wafer as claimed in claim 2 wherein the step of providing the compound semiconductor wafer includes providing a compound semiconductor wafer of indium-phosphide (InP).

5. A method of coating the surface of a compound semiconductor wafer structure as claimed in claim 1 wherein the step of providing the compound semiconductor wafer structure includes providing a compound semiconductor wafer with a semiconductor device formed thereon.

6. A method of coating the surface of a compound semiconductor wafer structure as claimed in claim 6 wherein the step of providing the compound semiconductor wafer structure includes providing a compound semiconductor wafer with a semiconductor integrated circuit formed thereon.

7. A method of coating the surface of a compound semiconductor wafer structure as claimed in claim 1 wherein the step of positioning a crystalline, high purity Ga_2O_3 evaporation source includes using a pure metallic iridium crucible that is generally of a conical shape having one closed end and one open end and has been fabricated using the electroforming process.

8. A method of coating the surface of a compound semiconductor wafer structure as claimed in claim 1 wherein the step of positioning a crystalline, high purity Ga_2O_3 evaporation source includes positioning the metallic iridium crucible in an effusion cell.

9. A method of coating the surface of a semiconductor wafer as claimed in claim 1 wherein the step of providing the compound semiconductor wafer includes providing a compound semiconductor wafer of gallium-arsenide.

10. A method of protecting the surface as claimed in claim 2, wherein crystalline gadolinium gallium garnet, $Ga_3Gd_5O_{12}$, is utilized as the evaporation source for gallium oxide molecules.

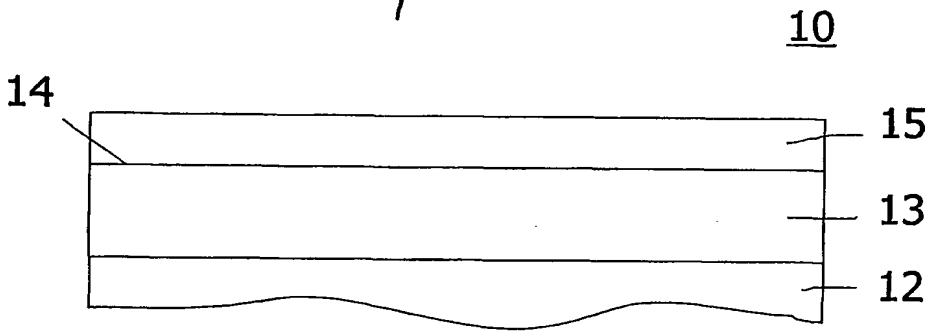

Figure 1

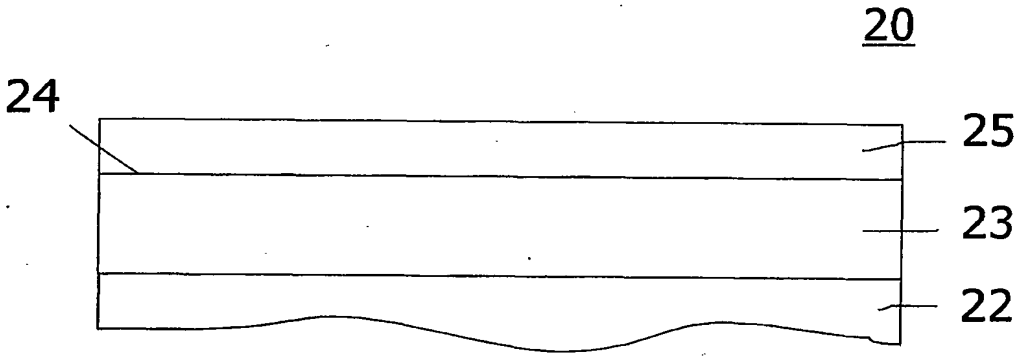

Figure 2

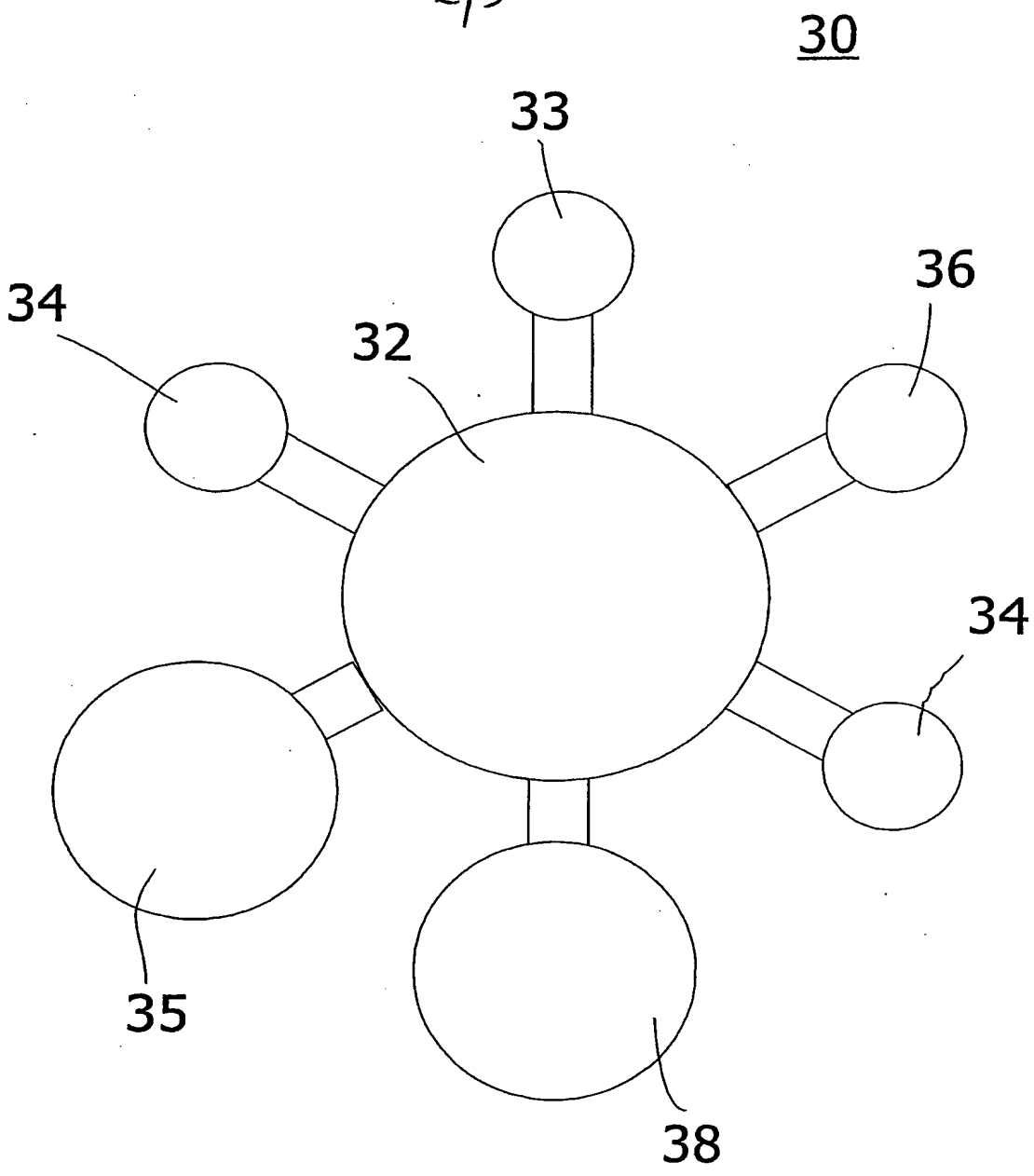

Figure 3

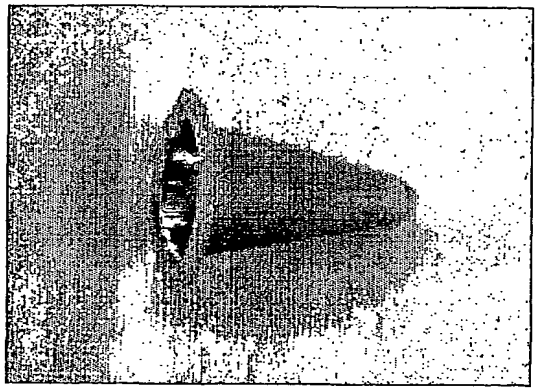

Figure 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/24263

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) :C30B 23/02; H01L 23/31
US CL :438/763, 761, 778, 779, 767, 481, 478
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/763, 761, 778, 779, 767, 481, 478

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

NONE

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6,030,453 A (PASSLACK et al) 29 February 2000 (29.02.2000), see entire document.	1-10
Y	US 6,094,295 A (PASSLACK et al) 25 July 2000 (25.07.2000), see entire document.	1-10
A	US 4,802,180 A (BRANDLE, JR. et al) 31 January 1989 (31.01.1989), see entire document.	1-10
Y	US 5,451,548 A (HUNT et al) 19 September 1995 (19.09.1995), see entire document.	10
Y	US 4,561,915 A (MITO) 31 December 1985 (31.12.1985), see entire document.	3, 4
Y	JP 8-85873 A (YOSHIZAWA) 02 April 1996 (02.04.1996), see entire document.	1-10

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

* Special categories of cited documents:

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Date of the actual completion of the international search	Date of mailing of the international search report
13 SEPTEMBER 2001	29 OCT 2001
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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/24263

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 6,006,582 A (BHANDARI et al) 28 December 1999 (28.12.1998), see entire document.	1-10